SLIC Switcher Circuit

Advanced
Micro
Devices

Application Note

The purpose of this application note is to present a description of the switched mode power regulator on the AMD® Am795XX/Am79M5XX family of Subscriber Line Interface Circuit (SLIC) devices. Based on analysis, suitable external components required by the SLIC are recommended, which guarantee stable switcher operation over a wide range of battery and load conditions.

FUNCTIONAL DESCRIPTION

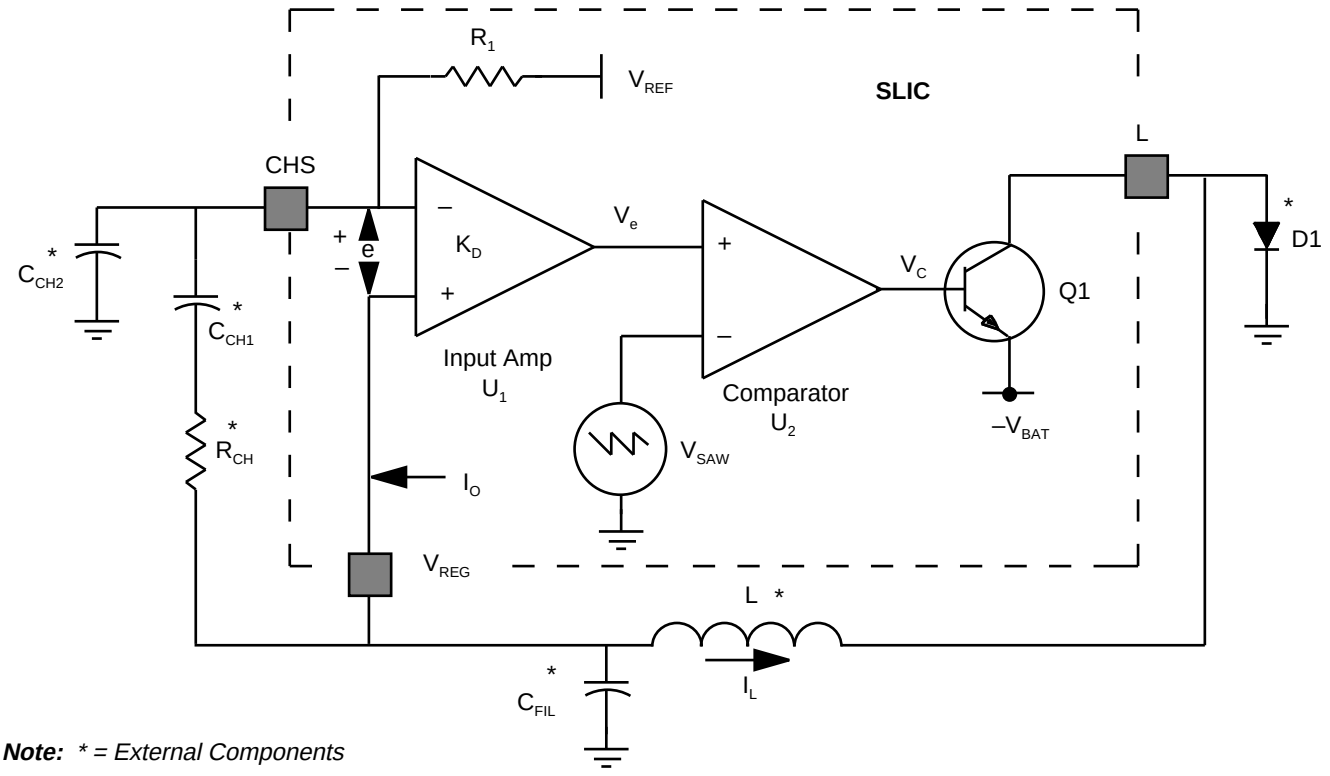
The purpose of the switched mode regulator or "switcher" circuit is to minimize power dissipation in the system by providing the power amplifier circuits of the SLIC with the minimum voltage required for proper operation. The switcher itself uses almost no power because it contains only an on-off switch and reactive components.

The switcher regulates the amplifier supply voltage, V_{REG}, such that it is always several volts more negative than the most negative SLIC output line (the "B" wire for normal polarity), but more positive than the battery voltage. Since the switcher is a high-efficiency power conversion device, this results in reduced power consumption for both the SLIC device and the system.

Figure 1 shows the equivalent circuit of the switcher. Components R_{CH}, C_{CH1}, C_{CH2}, C_{FIL}, and L and catch diode D1 are external components. All other components are internal to the SLIC device. The switcher output voltage, V_{REG}, is compared to voltage, V_{REF}, an internally generated voltage that is approximately twice the average of the longitudinal voltages at A and B, plus a small offset voltage. This guarantees that V_{REG} is always larger than VA – VB. An error voltage, e, is produced such that:

$$e = V_{REF} - V_{REG}$$

This voltage is amplified by differential input amplifier, U_1, and compared to the sawtooth voltage, V_{SAW}, by comparator U_2. A pulse is produced at the collector of Q1, whose duty cycle is proportional to error voltage, e. The pulse at pin L is smoothed by the filter formed by L and C_{FIL}, leaving an average DC voltage along with a small AC-ripple voltage at pin V_{REG}.



Note: ** = External Components*

Figure 1. SLIC Switcher Control Loop

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To simplify the following discussion, let us initially assume that C_{FIL} is 0 and the inductor L is large enough to act like an integrator and produce the idealized linear ramp voltage and current curves shown by V_e' and I_L' in Figure 2a and Figure 2c.

When V_e' is greater than V_{SAW} (see Figure 2a), V_C is positive and transistor Q1 turns on and switches inductor L to $-V_{BAT}$. The current I_L', flowing out of the V_{REG} node (see Figure 1), increases and hence V_{REG} drives negative until the sawtooth resets. At this time, V_{SAW} becomes greater than V_e' and Q1 switches off. Current in the inductor flows to ground through diode D1 and decreases in magnitude causing V_{REG} to drive positive until V_e is again greater than V_{SAW} and V_e' is again positive. In the above manner, the average value of V_{REG} follows V_{REF}.

Until now, a large inductor and no filter capacitor have been assumed. With real components, the voltage and current waveforms are shown by curves for V_e and I_L in Figure 2a and Figure 2c. The ripple voltage waveform V_e is shifted 180° as would be expected at the output of a two pole L-C filter at a frequency far above cut-off. The ripple current I_L leads the voltage by 90°, as it must, since it flows entirely through filter capacitor, C_{FIL}.

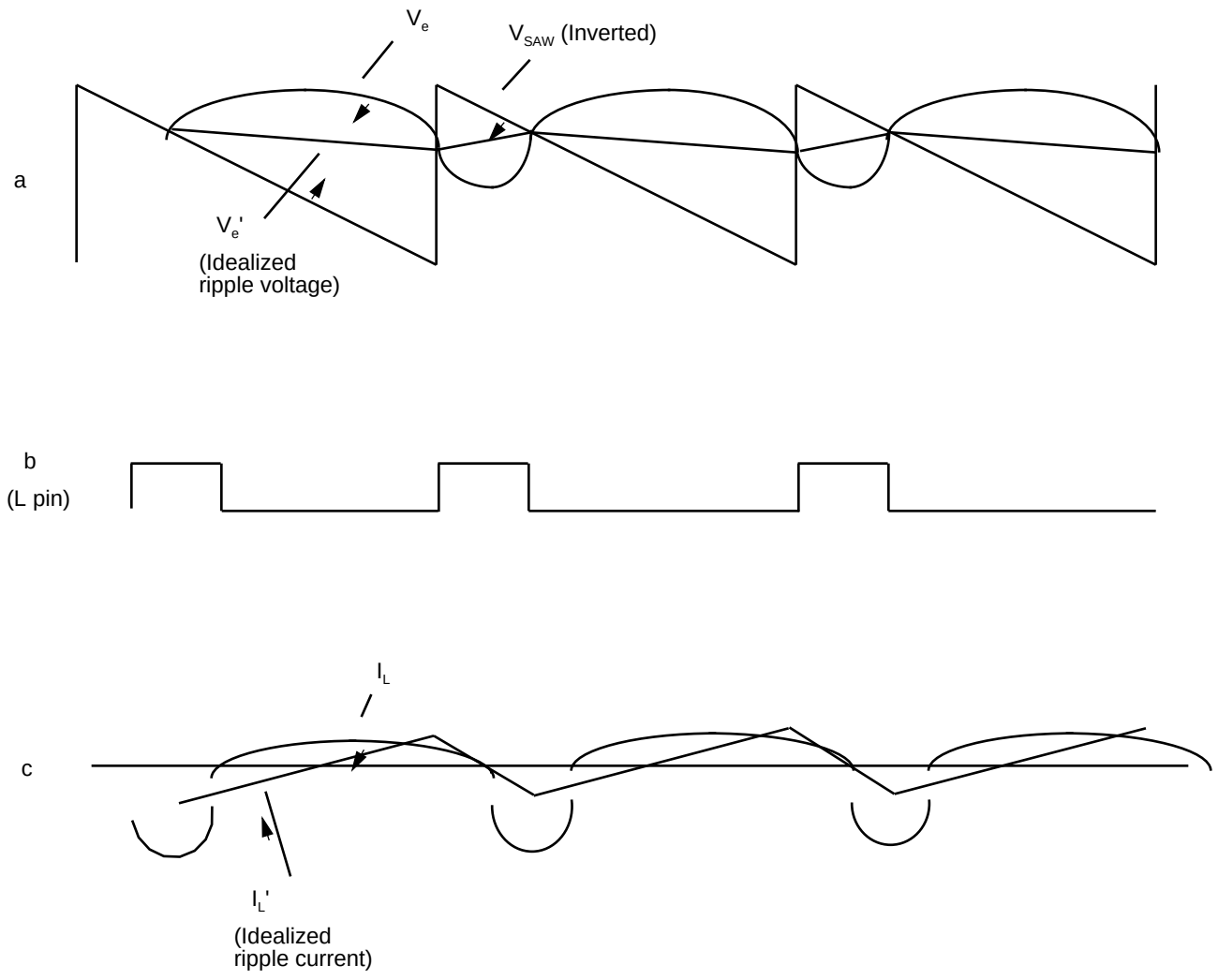

Figure 2. Switcher Voltage and Current Waveforms

Design Analysis

L-C Filter

The L-C filter is comprised of inductor L and capacitor C_{FIL} (see Figure 1) and is used to filter out the high frequency components of the variable duty cycle pulse produced by switching transistor Q1 and diode D1. The resulting V_{REG} is a DC level equal to the average voltage of the pulse plus a small amount of 256-kHz (CHCLK) ripple. It is critical that the ripple be kept as low as possible to ensure proper switcher operation and low noise in the voice channel. It is particularly important that the amount of possible 128-kHz ripple be kept low because, as will be shown, the switcher can revert to half-frequency switching if the attenuation of the filter at 128 kHz is insufficient.

The normal ripple voltage waveform at 256 kHz is shown in Figure 3. In this case, voltage X, plus the average voltage is below every sawtooth peak. Therefore, the switcher cannot operate at 128 kHz.

Figure 4 shows what can occur when the potential peak ripple at 128 kHz is too large. In this case, X is large enough such that V_{REG} waveform cannot intersect every sawtooth but will intersect every other sawtooth. The switcher will then operate at half frequency as shown. This effect is particularly evident in long loop situations when the average voltage is near the sawtooth peak. When the recommended component values are used, the series components R_{CH} and C_{CH1} reduce any potential 128-kHz ripple to a sufficiently low level to prevent half-frequency operation.

There is no gross difference in power consumption between the two frequencies of operation since the average value of V_{REG} is regulated by the control loop to remain the same in both cases. The problem occurs when, because of a particular load and battery condition, the switcher operates at the boundary between 128 and 256 kHz. Large amounts of noise can then be introduced into the voice channel as the switcher randomly finds one or the other frequency modes at which to operate. Another effect is that loop stability could be adversely affected because the effective sample and hold rate is now 128 kHz, (half as often), adding extra sampling delay in the loop.

Loop Stabilization

An important requirement in any control loop is that it is stable and free of any oscillations. Oscillations in the SLIC switching regulator can cause large amounts of noise on its own and on adjacent telephone lines. It can also cause device overheating and, if severe enough, the disabling of the entire line circuit.

In order to verify the stability of the overall switcher circuit, we must first derive the equations describing the control loop. After this, a Bode plot showing open loop gain and phase versus frequency can be drawn to establish the closed loop stability margins.

The overall configuration of the switching regulator control loop is shown in Figure 5. This functional schematic shows the following essential elements required to accurately define the small signal performance of the loop:

1. K_0 represents the low frequency gain of the input differential amplifier and the sawtooth comparator that results in the variable duty cycle pulse.
2. The sample and hold block simulates the filtering action caused by the average value of V_{REG} being effectively updated only after one complete cycle of the variable duty cycle signal at the output of K_0.
3. L and C_{FIL} are the elements that filter the pulse and provide a low ripple DC voltage at V_{REG}.
4. R_1, an internal resistor on the SLIC device, and external components R_{CH}, C_{CH2}, and C_{CH1} are used to shape the open loop gain and phase response.
5. R_S represents the effective series resistance of the inductor plus a resistance representing the loss in the catch diode and switching transistor.

   The derived Loop equations are shown in the appendix. A discussion of recommended components and selection criteria are presented before the results.

WAVEFORMS AT SAWTOOTH COMPARATOR INPUT

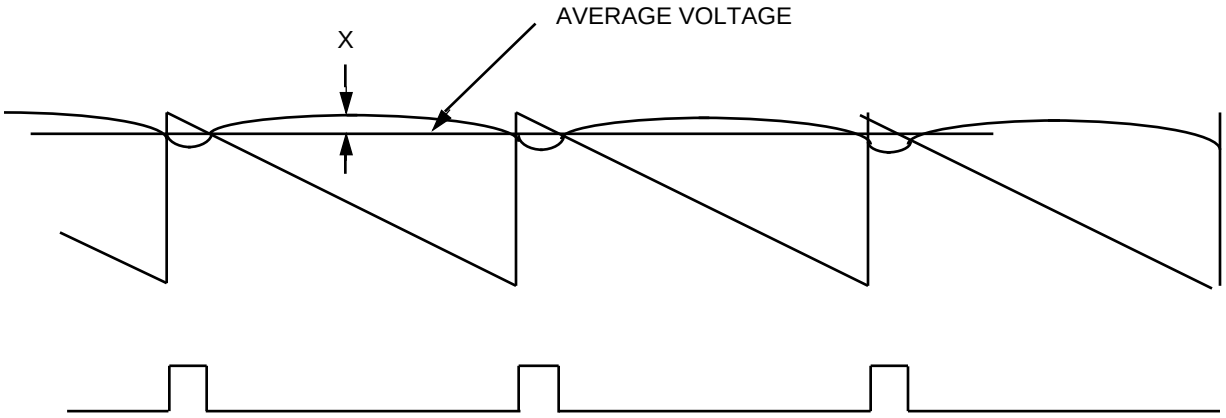

Figure 3. 256-kHz Mode

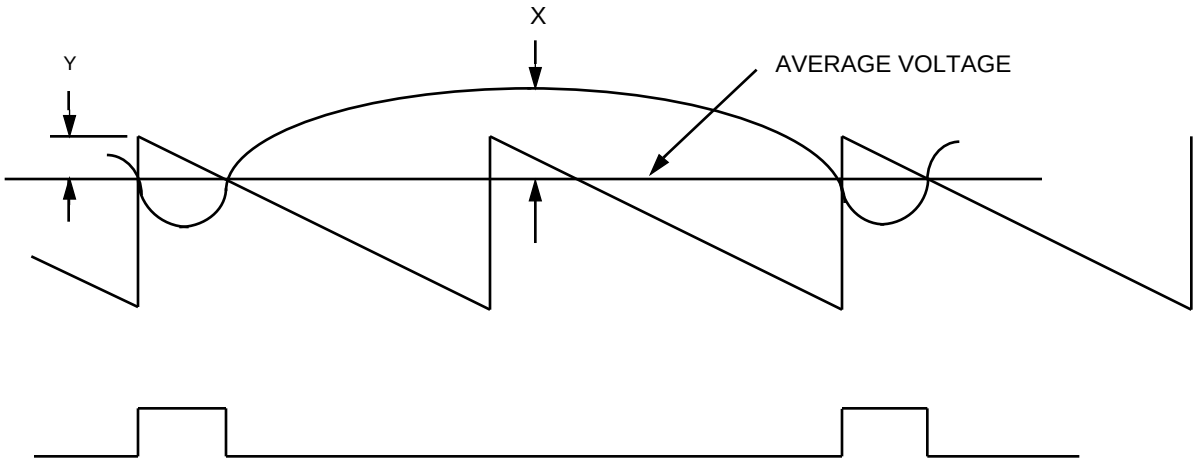

Figure 4. 128-kHz Mode

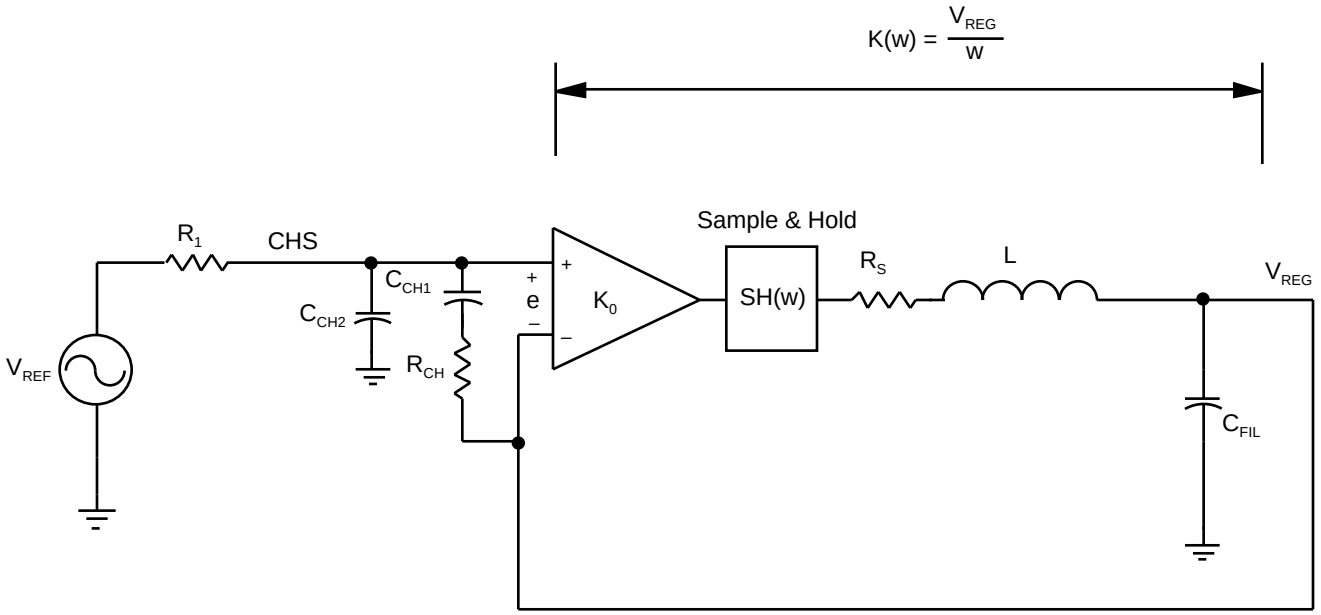

Figure 5. Small Signal Equivalent Circuit SLIC Switcher Control Loop

Recommendations

To eliminate the potential for half-frequency operation and to maintain adequate stability margins, the following switcher component values are recommended:

$L = 1$ mH

$C_{FIL} = 0.47$ µF

$C_{CH1} = 15$ nF

$C_{CH2} = 560$ pF

$R_{CH} = 1.3$ kΩ

Note: *The AMD SLIC devices include a circuit that disables the switcher for long loops to further reduce the possibility of half-frequency operation. Even under this condition, the above values of components should still be adhered to for optimum performance.*

Component Selection

Inductor, L

The inductor must be of a type that will lose a minimum amount of inductance when worst-case DC average plus peak 256-kHz AC ripple is flowing through the inductor. A solenoid type inductor similar to the J.W. Miller 73F series is recommended. This inductor has a high enough current rating to keep it out of core saturation. As an example, assume a 1-mH inductor and a .47-µF capacitor are used as the filter components. The ripple component of V_{REG} is:

$$V_{peak\ ripple} = \frac{2}{\pi} \bullet H_f \bullet V_{BAT}$$

where: H_f = Attenuation of the L-C filter

At 128 kHz and a maximum possible V_{BAT} of 64 V:

$$V_{peak\ ripple} = \frac{2}{\pi} \bullet 3 \bullet 10^{-3} \bullet 64 = 0.122\ \text{V}$$

$$I_{peak\ ripple} = C_{FIL}\ \frac{dV_{REG}}{dt}$$

$$= 0.47\text{E}{-6} \bullet 2\pi \bullet 128000 \bullet 0.122 = 46\ \text{mA}$$

The maximum DC current (I_{DC}) is limited by the SLIC device to 60 mA. The maximum DC plus peak ripple is then:

$$I_{peak\ max}(I_{peak}\ \text{AC} + \text{IDC} = 60 + 46 = 106\ \text{mA})$$

The J.W. Miller 1-mH inductor has a maximum current for rated inductance of 150 mA and therefore is acceptable for this application.

An inductor other than the one recommended above could be used. A note of caution is that the series resistance should be less than 20 Ω to ensure low power loss. On the other hand, a very low series resistance could have the effect of causing oscillation at the frequency where the inductor resonates with C_{FIL}. It is recommended that a Bode plot be run using the actual parameters to verify loop stability.

Inductors also have interwinding capacitance that creates a parasitic capacitor. The inductance will resonate with this capacitance. If this is at a sufficiently high frequency it will not affect the application, but one must account for this source of phase shift when determining stability of the loop.

Capacitor, C_{FIL}

The capacitor must be a good quality polyester film type with at least a 100-V rating that will maintain its value over the applied DC-voltage range and have a low effective series resistance (ESR) of less than half of the capacitive reactance at frequencies higher than 128 kHz. Because of cost and size considerations, values should be limited to below 0.47 μF @ 100 VDC. Many ceramic capacitors in this value range have severe capacitance reductions with increasing applied voltage. A reduction in capacitance can cause half-frequency operation due to insufficient filtering of the 128-kHz ripple. The overall loop stability can also be affected.

Measurements were made on various types of capacitors to determine the performance at 128 kHz over a 0- to 35-V DC-voltage bias. Figure 6 shows that the polyester film type has the advantage over the physically smaller, less expensive ceramic types. It loses none of its capacitance as voltage is increased as opposed to almost 50% loss for ceramics. The ESR is also the lowest. For these reasons, a 0.47 μF polyester or similar good quality capacitor is strongly recommended for use in the switcher filter circuit.

Capacitors C_{CH2} and C_{CH1} and Resistor R_{CH}

These are the components that perform the stabilizing function for the loop and that must be stable in order to maintain loop stability margins for worst-case conditions.

Capacitor C_{CH2} is connected between pin CHS and ground and is subjected to DC-bias voltages of up to 60 V depending on the SLIC device. It is important that this capacitor be as stable as possible because of its influence on half-frequency operation as well as the loop stability. A 10% tolerance ceramic with an X7R temperature stability characteristic is recommended because of its stability and immunity to DC-bias changes.

Capacitor C_{CH1} must also be relatively stable. A 10% tolerance ceramic capacitor with an X7R temperature characteristic will be satisfactory though the voltage rating must be able to withstand at least the battery voltage.

Use of ceramic capacitors designed primarily for bypassing with EIA Z5U stability characteristics must be avoided. According to published data, they can exhibit up to a 66% reduction in capacitance from their nominal value due to tolerance and temperature effects. With these large variations, the loop can become unstable under worst-case conditions.

The value of resistor R_{CH}, as with C_{CH2}, affects half-frequency operation as well as stability and should be a 2% film type.

Results

Using the derived equations that are in the appendix and the recommended values above, a Bode plot (open loop gain and phase versus frequency) can be generated that reveals the stability margin when the loop is closed. Figure 7 shows the Bode plot for the switcher control loop using the component values recommended above and the maximum calculated gain, K_0, of 169 at $V_{BAT} = -48$ V. A short circuit loop was also assumed since this gives lowest switch resistance tending to make the loop less stable. The gain and phase margins show that, with these values, the gain margin is 9.5 dB and the minimum phase margin is 20°.

The minimum phase margin occurs at frequencies where L resonates with C_{FIL}. This phase margin is independent of the gain of the system and can vary with component tolerance. Phase margin at this frequency can also be increased by using an inductor with a higher series resistance as long as the resistance is not so high as to cause excessive DC voltage drop and the inductor does not saturate because of insufficient core area.

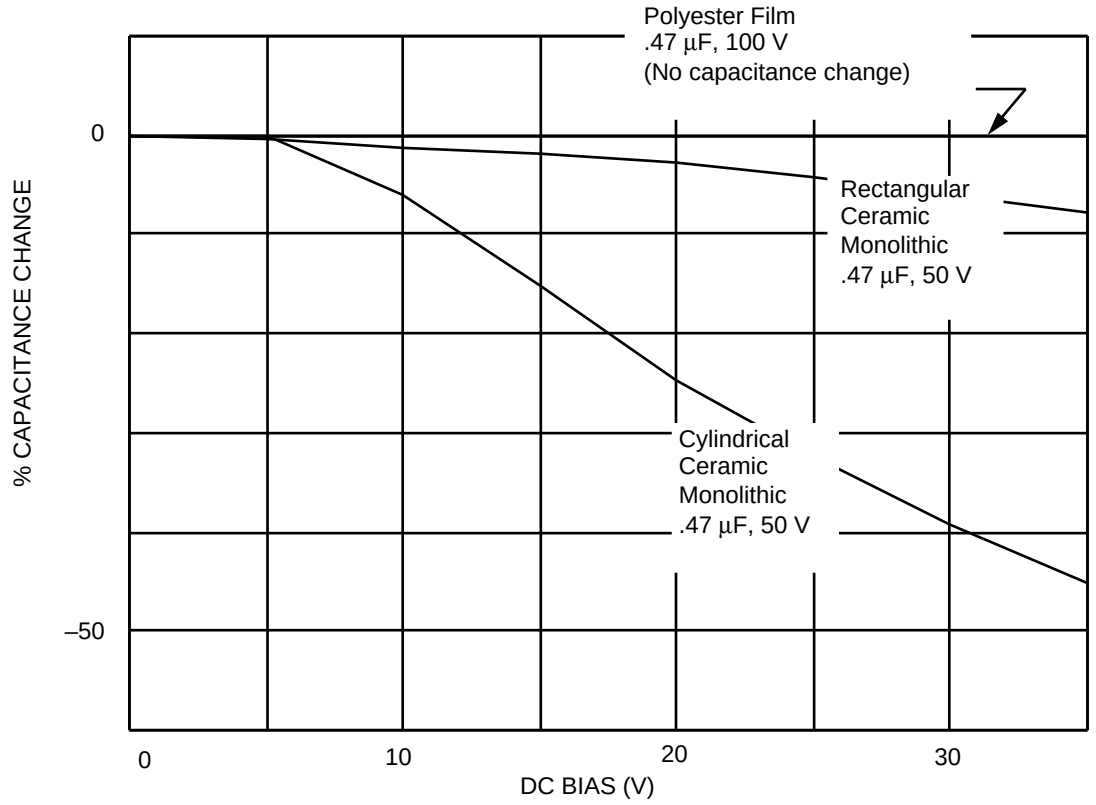

Figure 6. Capacitor Variation vs. Voltage

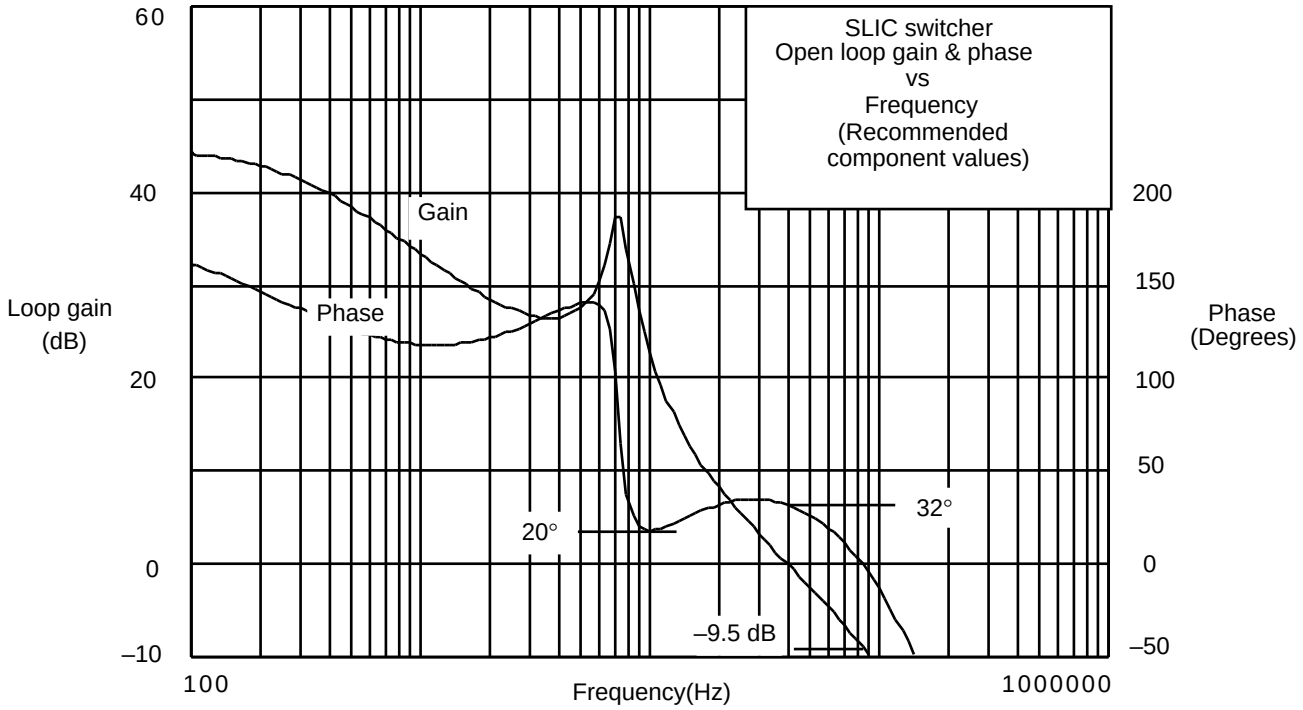

Figure 7. Open Loop Gain and Phase vs. Frequency

Appendix: Derived Loop Equation

Referring to Figure 5, the equation for the closed loop gain from VREF to V_{REG} is:

$$GCL(w) = \frac{1 + jwT_2}{1 - w^2T_1T_2 + jw(T_1 + T_2 + T_3)} \quad K(w)/1 + K(w)\frac{(1 + jwT_1)\ (1 + jwT_2)}{1 - w^2T_1T_2 + jw(T_1 + T_2 + T_3)} \qquad \text{Eq. (1)}$$

where: $T1 = R_1C_{CH2}$

$T2 = RC_HC_{CH1}$

$T3 = R_1C_{CH1}$

$K(w) = \frac{VREG(w)}{e(w)}$

Equation 1 is of the form:

$$GCL(w) = Gin(w)\frac{K(w)}{1 + K(w)H(w)} \qquad \text{Eq. (2)}$$

This is the familiar expression for the gain of a closed loop system modified by the term Gin(w) representing the input filtering effect of R1. K(w) is the amplifier gain function and H(w) is the feedback function.

Comparing Equation 2 to Equation 1:

$$H(w) = \frac{(1 + jwT_1)(1 + jwT_2)}{1 - w^2T_1T_2 + jw(T_1 + T_2 + T_3)} \qquad \text{Eq. (3)}$$

K(w) includes the low frequency gain, K_0, multiplied by the sample and hold and L-C filter responses:

$$K(w) = H_0\ V_{BAT} \bullet \frac{\text{Sin}\frac{wT_s}{2}}{\frac{wT_s}{2}} \left(\text{Cos}\frac{wT_s}{2} - j\text{Sin}\frac{wT_s}{2}\right) \bullet \frac{1}{1 - w^2LC_{FIL} + jw(R_SC_{FIL})} \qquad \text{Eq. (4)}$$

K_0 Sample & Hold L-C filter

H_0 = Factor accounting for input amplifier gain and sawtooth slope

(Nominal value = 1.86 V^{-1})

T_s = Sample period ($4 \bullet 10^{-6}$ for the 256-kHz switcher frequency)

In Equation 4, R_S is a resistance representing the inductor and switch resistances and has a considerable effect on the stability of the loop. The inductor series resistance can be measured or obtained from a data sheet for the inductor. The switch resistance can be a significant part of the total and consists of AC resistance of diode D_1 when Q_1 is off, and the saturation resistance of transistor Q_1 when it is on. The total switch resistance averaged over a full cycle is then:

$$R_{SW} = D\frac{V_T}{I_L} + (1 - D)R_{SAT}$$

Where: D = Pulse duty cycle (load dependent)

V_T = 0.026 V for a silicon diode

$R_{SAT} \approx 5.5\ \Omega$

The total resistance is: $R_S = R_{INDUCTOR} + R_{SW}$

The open loop gain is obtained by multiplying Equation 3 and Equation 4:

$G_{OL} = K(w)H(w)$

This is the equation used to generate the Bode plot of Figure 6.